ME 103 Experimentation and Measurements
Spring 2026 George Anwar

HW0

Due: Monday, January 26 at 11:59 pm

- This homework will review required electronics knowledge covered in ME100.
- In all of the questions, **show your work**, not just the final answer. Unless we explicitly state otherwise, you may expect full credit only if you explain your work succinctly, but clearly and convincingly. For coding questions, attach a screenshot of your code and output.
- Present your answers with **a suitable number of significant figures** for each question. Show your work, including a mathematical formula or redrawn circuits. Appendix B has all the rules and examples for significant digits.
- Treat all diodes and Zener diodes as ideal, unless otherwise stated. Assume each operational amplifier is supplied with a ±9V voltage source, unless otherwise stated, which is also the op-amp output range. Finally, assume that, in a transistor, the voltage drop between the base and the emitter is 0.6V and the voltage drop between the collector and the emitter is 0V if the transistor is saturated.
- If you have a confirmed disability that precludes you from complying fully with these instructions or with any other parameter associated with this problem set, please alert us immediately about reasonable accommodations afforded to you by the DSP Office on campus.
- **Start early. This material is prerequisite material not covered in lecture; you are responsible for finding resources to understand it.**

Deliverables

Submit a PDF of your homework to the **Gradescope assignment** entitled "{Your Name} HW0". You **must** typeset your homework in LaTeX (submit PDF format, not .doc/.docx format) . Mac Preview, PDF Expert, and FoxIt PDF Reader, among others, have tools to let you sign a PDF file. We want to make *extra clear* the consequences of cheating.

1 Honor Code

I will adhere to the Berkeley Honor Code: specifically, as a member of the UC Berkeley community, I act with honesty, integrity, and respect for others. Failure to comply with these guidelines can be considered an academic integrity violation. Please email Professor Anwar ganwar@berkeley.edu if you have any questions!

- **List all collaborators. If you worked alone, then you must explicitly state so. Read the following statement and sign below if you agree**:

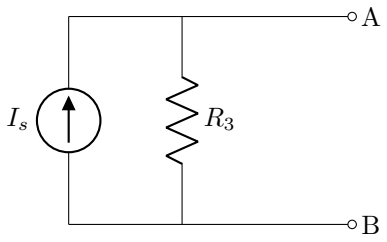
  "I certify that all solutions in this document are entirely my own and that I have not looked at anyone else's solution. I have given credit to all external sources I consulted."

  Signature : _____ *Date* : _____

  While discussions are encouraged, *everything* in your solution must be your (and only your) creation. Furthermore, all external material (i.e., *anything* outside lectures and assigned readings, including figures and pictures) should be cited properly. We wish to remind you that consequences of academic misconduct are *particularly severe*!
- Violation of the Code of Conduct will result in a **zero** on this assignment and may also result in disciplinary action.

2 Thévenin and Equivalent Circuits [20 pts]

A $4-20$ mA pressure transmitter is being interfaced to a data acquisition system (DAQ). Over the frequency range of interest, the transmitter can be modeled as an ideal Norton current source I_s in parallel with an internal resistance R_3. Terminals $A-B$ are the transmitter output terminals that connect to your measurement input. A circuit diagram is shown below:

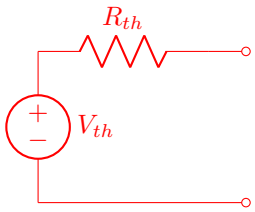


1. [2 pts] Draw the Thévenin equivalent seen at terminals $A-B$ for a current source $I_s = 0.2A$ and $R_3 = 20\Omega$, and determine V_{th} and R_{th}.

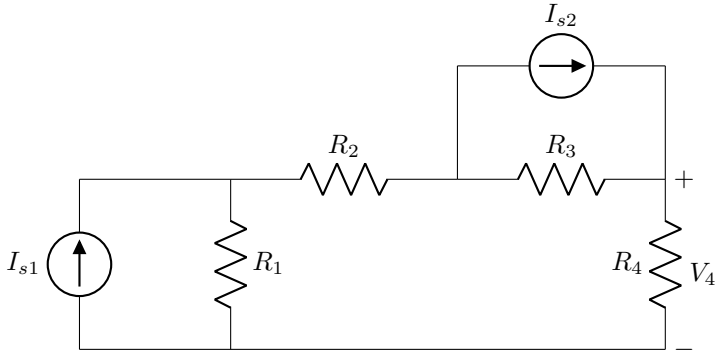
   Solution: This is a Norton equivalent circuit. Therefore, we can use $V_{th} = I_{no}R_{no}$ and $R_{th} = R_{no}$ to determine the Thévenin equivalent circuit

   $$V_{th} = V_{AB} = I_s R_3 = 4V, \quad R_{th} = R_3 = 20\Omega$$

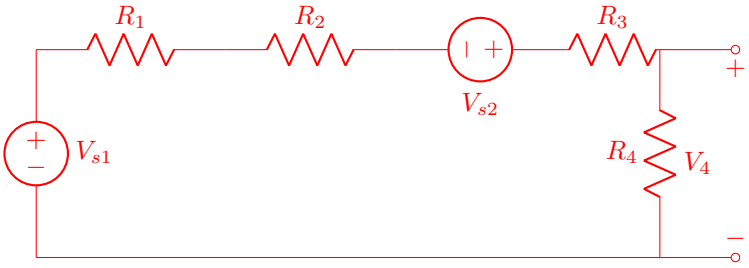
   The circuit is drawn as follows:



2. [5 pts] Now consider, a new circuit shown below. Redraw it bearing the following restrictions in mind: you can only use **two voltage sources** and the given **four resistors**. Determine the value of the voltage sources given $R_1 = 30\Omega$, $R_2 = 10\Omega$, $R_3 = 20\Omega$, $R_4 = 10\Omega$, $I_{s1} = 0.\overline{33}A$, and $I_{s2} = 0.2A$. **Do not combine resistors and you must include R_1, R_2, R_3, and R_4.**



Solution: Firstly, I_{s1} and R_1 is a Norton equivalent circuit so we can transform it into a Thévenin equivalent circuit. The same process can be done for I_{s2} and R_3. Therefore, the redrawn circuits.



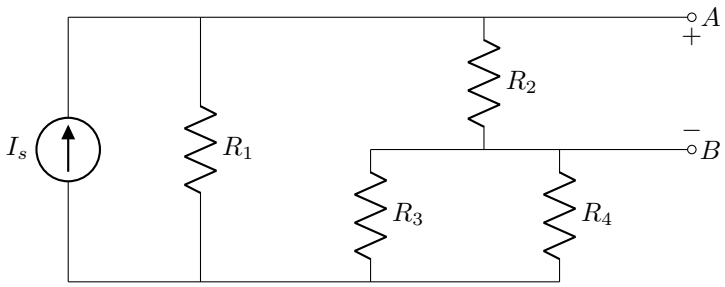
Therefore, the value of the voltage sources are $V_{s1} = I_{s1}R_1 = 10\text{V}$ and $V_{s2} = I_{s2}R_3 = 4\text{V}$.

3. [5 pts] Calculate the voltage drop across R_4.

Solution: Firstly, we combine the sources $V_{s1} + V_{s2} = 14\text{V}$. Then, note that we end up with a voltage divider, hence

$$V_4 = \frac{R_4}{R_1 + R_2 + R_3 + R_4}(V_{s1} + V_{s2}) = \frac{140}{70} = 2V$$

4. [8 pts] Consider a new circuit, find V_{th}, R_{th} with respect to nodes A and B for the following circuit in terms of the variables I_s, R_1, R_2, R_3, and R_4. You may leave the parallel operator $\|$ in your final answer.



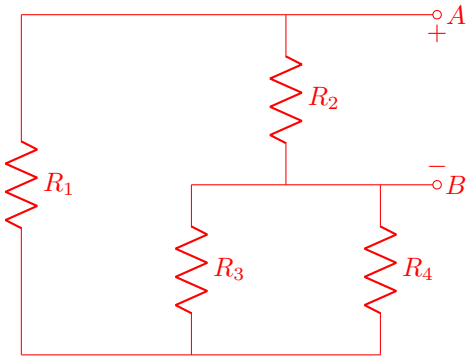
Solution: Note that the Thévenin voltage is across R_2. To fine the V_{R2} we need to first find the current through R_2 which we can simply apply the current divider formula

$$I_{R2} = \frac{R_1}{R_1 + R_2 + (R_3 \| R_4)} I_s$$

Then just by Ohm's law, we have

$$V_{th} = R_2 I_{R2} = \frac{R_1 R_2}{R_1 + R_2 + (R_3 \| R_4)} I_s$$

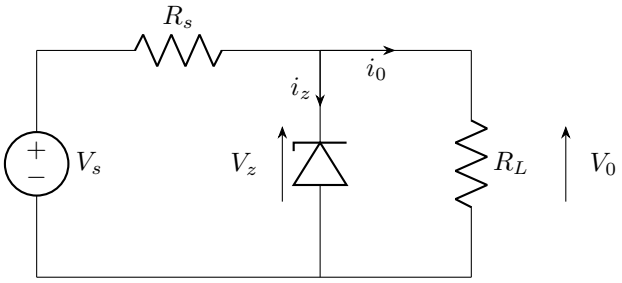
To find the Thévenin resistance, we begin by removing all independent source. The circuit is drawn below.



From this circuit, we can see the Thévenin resistance $R_{th} = R_2 \| (R_1 + (R_3 \| R_4))$.

3 Shunt Voltage Regulator [20 pts]

A Zener diode can be used to create a simple shunt voltage regulator to power a measurement device that requires a stable DC rail, as illustrated below:



In this measurement scenario, the regulated output V_0 is used to supply a sensor + signal-conditioning front-end (e.g., an instrumentation amplifier and ADC reference rail). The effective load seen by the regulator varies because the measurement system can switch operating modes (sleep/active, different gain settings, heater on/off, etc.), which changes the equivalent load resistance R_L.

1. [7 pts] Using KVL, KCL, and Ohm's law, derive an expression for the Zener diode current i_z as a function of the resistance R_s, the Zener voltage V_z, the input voltage V_s and the output current i_0.

   Solution: First, we can apply KVL in the left loop and we get

   $$V_s - V_{R_s} - V_z = V_s - i_s R_s - V_z = 0 \implies i_s = \frac{V_s - V_z}{R_s}$$

   Then, we can apply KCL at the top junction (above Zener diode) as follows

   $$i_s - i_o - i_z = \frac{V_s - V_z}{R_s} - i_0 - i_z = 0 \implies i_z = \frac{V_s - V_z}{R_s} - i_0$$

2. The voltage regulator circuit above is used to stabilize the voltage across a variable measurement load R_L, which can vary between $10 - 100\,\Omega$. The Zener diode is of type C9V4, with a maximum power rating of $7.5W$, and $V_s = 12V$.

   (a) [4 pts] Select the smallest value of R_S to protect the circuit when the load is disconnected.

   Solution: When the load is disconnected, $i_o = 0$. Also note that a Zener diode of type C9V4 means a Zener voltage of 9.4, thus

   $$i_z = \frac{12 - 9.4}{R_s}$$

   But note that $\max i_z = \frac{7.5}{9.4} = 0.8A \implies R_s = \frac{12-9.4}{0.8} = 3.3\Omega$ (2 s.f.)

   (b) [4 pts] With the value of R_s found in (a), what is the power dissipation of the variable load when R_L is 10, 50, and $100\,\Omega$?

   Solution: $i_{RL} = \frac{9.4}{R_L}$. If $i_{RL} \leq \max i_z$ this implies that the Zener diode is active for 50Ω and 100Ω, but not for 10Ω. From part (a), we determined the maximum current available through R_s is 0.8, but for $R_L = 10\Omega \implies i_{RL} = 9.4/10 = 0.94$A. So the load wants more current than the source can supply and thus the Zener cannot stay in breakdown. Hence, when the Zener is off, the circuit becomes 2 resistors so the laod voltage comes from a voltage divider:

   $$V_0 = \frac{R_L}{R_s + R_L} V_s \implies P_{10} = \frac{V_0^2}{R_L} = \frac{(\frac{10}{3.25+10} \times 12)^2}{10} = 8.2W = 8W$$

   $$P_{50} = \frac{9.4^2}{50} = 1.8W = 2W$$

   $$P_{100} = \frac{9.4^2}{100} = 0.9W$$

(c) [5 pts] Under these conditions, will this circuit be able to maintain the regulated voltage over the specified range of R_L? If yes explain why; if not explain what changes could be made to the circuit to make this possible.

Solution: The maximum current draw happens with the minimum load resistance:

$$\max i_o = \frac{V_z}{10} = 0.94\text{A}$$

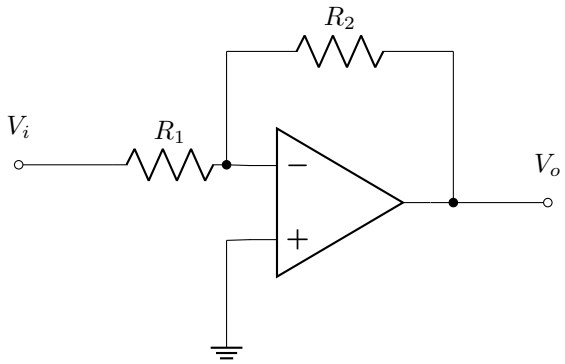
But the maximum current that can be delivered by the regulated supply is

$$i_{in} = \frac{V_s - V_z}{R_s} = 0.8\text{A}$$

As it occurs when i_z is zero. Thus, the circuit will not be able to maintain the regulated voltage of 9.4V over the specified range of $R_L = 10\Omega$. We would need to increase the power rating of the Zener diode.

4 Feedback Op-Amp [20 pts]

Consider the following op-amp stage employing feedback.



1. [3 pts] What is the name of this op-amp stage? Name one advantage and one disadvantage of this stage.

   Solution: This op-amp stage is an inverting amplifier. An advantage is that the gain can be less than 1. A disadvantage is a 180 degree phase shift

2. [4 pts] Demonstrate from first principles that the relationship between the input and output voltages for this stage is

$$V_o = -\frac{R_2}{R_1} V_i$$

   Solution: The non-inverting input (+) is grounded. Then assuming ideal op-amp and since it is in negative feedback, we have $V_+ = V_- = 0\text{V}$. Note that another golden rule is that current to the input pins of the op-amps are 0. Then, we can do nodal analysis at the node after R_1

$$\frac{V_i - 0}{R_1} = \frac{0 - V_o}{R_2} \implies \frac{V_i}{R_1} = -\frac{V_o}{R_2} \implies V_o = -\frac{R_2}{R_1} V_i$$

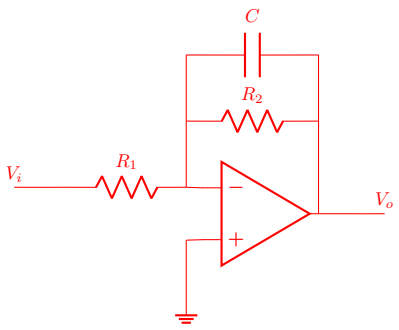
3. By adding a capacitor C in parallel with resistor R_2, the op-amp stage in the circuit above can be turned into an active low-pass filter, where the relationship between input and output voltages can be expressed in complex form as:

$$|H| = \frac{R_2}{R_1} \frac{1}{\sqrt{1 + (\omega R_2 C)^2}}, \quad \phi = 180^\circ - \arctan(\omega R_2 C)$$

   Assuming $R_1 = R_2 = 1000\Omega$:

   (a) [5 pts] Sketch the circuit and compute $|H|$ and ϕ when the output power is half of the power of the input signal, and when the input signal is DC.

   Solution: The circuit is as follows



For a resistive load, the power is just V^2/R. So if we take the ratio of output and input power we have

$$\frac{P_o}{P_i} = \frac{V_o^2/R}{V_i^2/R} = \left(\frac{V_o}{V_i}\right)^2$$

And by definition, the magnitude of a transfer function is the voltage ratio so $|H(j\omega)| = |V_o|/|V_i| \implies P_o/P_i = |H(\omega)|^2$. So half power means $P_o/P_i = 0.5 \implies |H|^2 = 0.5 \implies |H| = 1/\sqrt{2}$. This is exactly the -3db cutoff. To solve for the phase, we have

$$\frac{1}{\sqrt{1+(\omega R_2 C)^2}} = \frac{1}{\sqrt{2}} \implies 1+(\omega R_2 C)^2 = 2 \implies \omega R_2 C = 1$$

Then

$$\phi = 180^\circ - \arctan(1) = 180^\circ - 45^\circ = 135^\circ$$

When the input signal is DC, this means that $\omega = 0$. So

$$|H(0)| = \frac{1}{\sqrt{1+0}} = 1,\ \phi(0) = 180^\circ - \arctan(0) = 180^\circ$$

(b) [5 pts] If V_i is produced by a constant 5V voltage source able to deliver a maximum current of 2mA, choose a value of C that would ensure the filter attenuates 50Hz humming noise by 20dB and compute V_0.

Solution: If the input voltage source has a maximum current value, it must be real, with internal resistance

$$R_s = \frac{5}{0.002} = 2500\Omega$$

For 20dB attenuation at 50Hz i.e. $|H(50\text{Hz})|_{dB} = -20$, we have

$$-20 = -20\log_{10}\left(\frac{50}{f_c}\right) \implies 10 = \frac{50}{f_c} \implies f_c = 5\text{Hz}$$

This could also be done knowing that a 1st order LPF has one pole in its transfer function so we lose 20db/decade. Hence, after 20db, we reduce the magnitude by a factor of 10. Now, for the inverting active LPF,

$$f_c = \frac{1}{2\pi RC} \implies C = \frac{1}{2\pi(1000)(5)} = 31.8\,\mu\text{F}$$

Because of the source resistance, the DC gain is no longer $-R_2/R_1 = -1$. The gain of the filter is now seen as a voltage divider

$$|H|_{DC} = \frac{1000}{2500+1000} = 0.29$$

and the input is inverted:

$$V_o = 5 \times 0.29 \times -1 = -1.43V$$

Note: you could consider $|H|_{DC,dB} = 20\log_{10}(0.29) = -10dB$ in the calculation of f_c. Then, the attenuation at 50Hz should only be 10 dB, $f_c = 17$Hz, $C = 9.55\,\mu$F and $|H|_{DC}$ stays the same; you would get full points anyways.

(c) [3 pts] Why can active filters be used more easily in series than passive filters?

Solution: Active Filters use powered components to filter a frequency. It can be placed in series with other circuit components without the voltage entering the circuit being changed due to its high input impedance and low output impedance. A passive filter has no protection against this, meaning circuit components will change the voltage of the circuit and subsequently shift the cutoff frequency of the filter

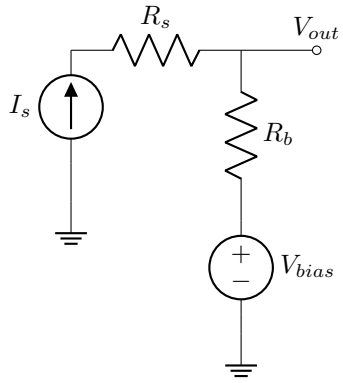
It also makes calculations easy i.e. you can multiply stage transfer functions.

5 Data Conversion Circuits [22 pts]

In many measurement systems, sensors produce small analog signals (often currents or voltages) that must be biased, amplified, digitized, and combined before a microcontroller/DAQ can use them. The following circuits are common building blocks in measurement instrumentation (e.g., photodiodes, ionization sensors, piezoelectric sensors, strain/bridge readout, and DAQ front ends).

(a) [4 pts] In optical measurement systems such as ambient light monitoring or optical power meters, a **photodiode** converts incident light into an electrical current proportional to light intensity. Over its operating range, the photodiode can be modeled as a current source I_s.

In many lab setups, we need to shift the DC operating point of the photodiode output so that the measured voltage,V_{out}, falls within the input range of a data acquisition system (DAQ) or oscilloscope. One way we can do this is by injecting a bias voltage V_{bias} through a resistor at the receiver side. Consider this simple photodiode readout circuit:

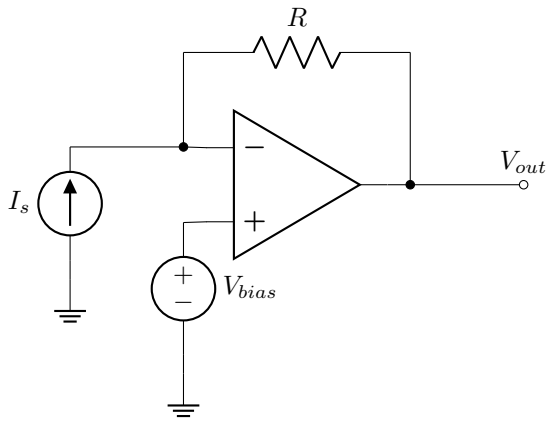


Using **superposition**, solve for the voltage V_{out} in terms of I_s, V_{bias}, R_s, and R_b. Show your work.

Solution: Firstly, let's turn off the current source and keep the voltage source on. The circuit is an open circuit now, so $V_{out,1} = V_{bias}$. Then, keep the current source on and turn the voltage source off, the current in the circuit is I_s so $V_{out,2} = I_s R_b$. Therefore, by superposition

$$V_{out} = V_{out,1} + V_{out,2} = V_{bias} + I_s R_b$$

(b) [4 pts] The previous sensor interface may have issues with loading. A common fix in measurement systems is to use an op-amp that converts sensor current into voltage while presenting a controlled input condition to the sensor. Consider the op-amp circuit shown:

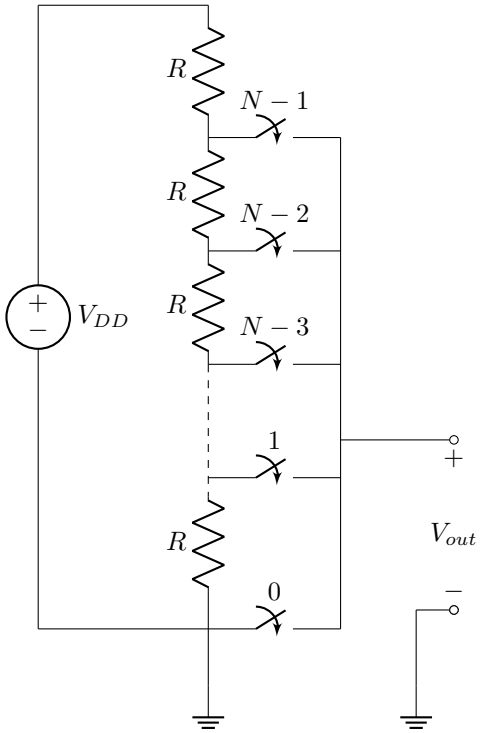


Calculate the voltage at the output V_{out} in terms of I_s, V_{bias}, and R. Show your work. You will not receive **credit** for directly copying a known formula.

Solution: By the golden rules of op-amps, all the current I_s goes through the feedback resistor R, so the voltage drop on the resistor is $V_R = -I_s R$. From our golden rules as well, the voltage of the negative terminal of the op-amp must also be equal to V_{bias}. Therefore

$$V_{out} = V_{bias} + V_R = V_{bias} - I_s R$$

(c) [4 pts] Measurement systems often need a programmable analog voltage. That is, we need some circuit to allow us to convert between our analog voltage values and some digital representation stored as 1s or 0s. You will learn more about digital-to-analog converter (DAC) circuits in lecture! But, as preparation let's inspect one here. Consider the resistor-ladder DAC shown:



Note that there are N resistors and N switches in the circuit. Depending on some input digital code, one of the switches is closed, connecting the output to some node in the resistor ladder.

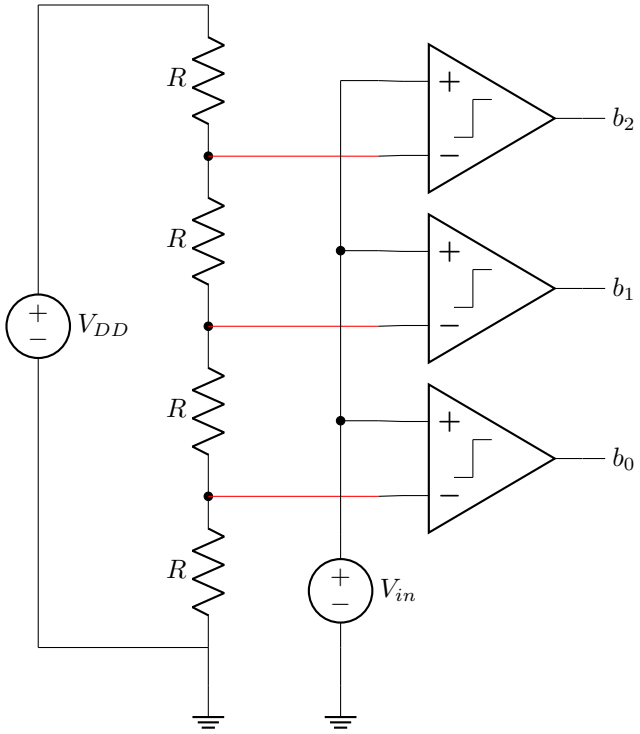
If only the ith switch is closed ($0 \leq i \leq N-1$), what is the output voltage V_{out} in terms of V_{DD}, i, N, and R?

Solution: We can divide the resistor ladder into a top and bottom, then count up the number of resistors we have that form the top and bottom.

$$\begin{aligned} V_{out} &= \frac{R_{bot}}{R_{top} + R_{bot}} V_{DD} \\ &= \frac{iR}{iR + (N-i)R} V_{DD} \\ &= \frac{i}{N} V_{DD} \end{aligned}$$

(d) [4 pts] The dual to DAC circuits are analog-to-digital converters (ADC). One simple measurement-oriented ADC concept is a flash-style front end, where a resistor ladder generates reference voltages and a bank of comparators determines where the input V_{in} falls relative to those references.

Consider the ADC circuit shown, using resistors and comparators:



Note: The red wires in the diagram are regular wires, but have been colored to show that they do not touch the crossing black wires.

The resistor ladder gives us a set of reference voltages to compare against. We use a set of comparators to compare the input voltage V_{in} against these reference levels, and we get out a corresponding digital code b_0, b_1, b_2.

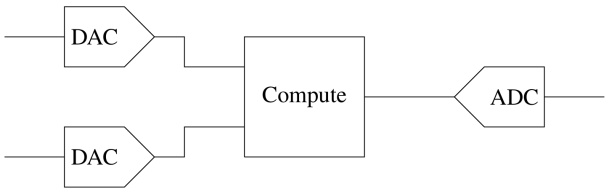
Assume that $V_{DD} = 1V$, and that the comparators are connected to rails $V_{DD} = 1V$ and $V_{SS} = 0V$. If V_{in} is $0.3V$, what are the outputs b_0, b_1, and b_2?

Hint: Each comparator checks if V_{in} is greater than the reference voltage, outputting V_{DD} if it is greater and V_{SS} if it is not. You may also look at the Appendix below for more information!

Solution: The reference voltages for the comparators, from bottom to top, are $\frac{1}{4}V_{DD} = 0.25\text{V}$, $\frac{1}{2}V_{DD} = 0.5\text{V}$, and $\frac{3}{4}V_{DD} = 0.75\text{V}$. Each comparator checks if V_{in} is greater than the reference voltage, outputing V_{DD} if it is greater than V_{ss} if not. We are given $V_{in} = 0.3\text{V}$, so $b_0 = V_{DD} = 1\text{V}$, $b_1 = V_{SS} = 0\text{V}$, $b_2 = V_{SS} = 0\text{V}$.

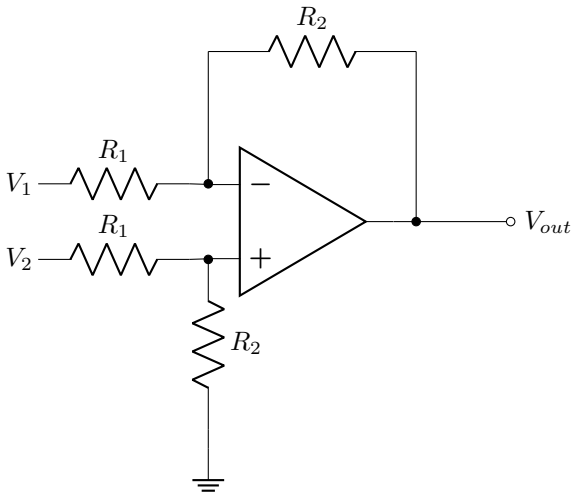
$$b_0 = 1, b_1 = 0, b_2 = 0$$

(e) [6 pts] DAC and ADC blocks help us represent numbers using voltage values. In many measurement systems, we also need analog front-end blocks that effectively compute before digitization. Examples include subtracting two sensor channels, scaling a difference, or combining signals to reject common-mode effects (noise, drift, supply variation).



This is also an example of analog computing! An example of this an artificial neuron circuit, now used as the hardware for Artificial Neural Networks (ANNs). These analog circuits could have massive speed benefits over their digital counterparts.

A classic example we will look at is the differential amplifier, widely used in instrumentation and sensor readout (e.g., taking the difference between two nodes of a bridge or between two measurement channels). It is also used in audio amplifiers and useful for mathematical computing.



From the above circuit, find the output V_{out} in terms of V_1, V_2, R_1, and R_2.

Solution: Let's approach this problem with superposition. First we turn off V_2 and keep V_1 on. Note that we have no current flowing through the resistors at the positive terminal, so we effectively have ground at that node. Thus, this is just an inverting amplifier:

$$V_{out} = -\frac{R_2}{R_1} V_1$$

Next, we turn off V_1 and keep V_2 on. We have two things happening in this circuit. The first pair R_1 and R_2 connecting V_2 to the positive terminal form a resistive voltage divider. Then the op-amp and the feedback R_1 and R_2 form a non-inverting amplifier:

$$V_{out} = \frac{R_2}{R_1 + R_2} \frac{R_1 + R_2}{R_1} V_2 = \frac{R_2}{R_1} V_2$$

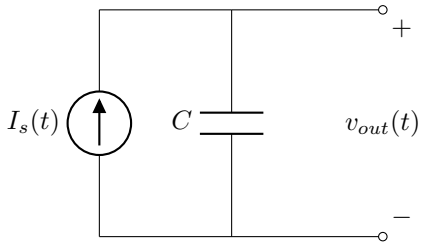
Adding these together, we get:

$$V_{out} = -\frac{R_2}{R_1} V_1 + \frac{R_2}{R_1} V_2 = \frac{R_2}{R_1} (V_2 - V_1)$$

6 Light Meter [18 pts]

Despite Professor Anwar's insistence that you were not allowed to create an automatic plant waterer, you have decided to ignore him! However, you forgot to consider sunlight! Your plants, despite getting enough water, keep dying. To prevent this, you have designed a circuit to measure the lights that the plant gets. We start with a photodetector which we simply model as a current source I_s. When the plants are getting sufficient exposure, the current source outputs 5 nA. Conversely, when they are *not* getting enough sun exposure the current source outputs 0 nA.

1. [6 pts] We set up the current source I_s as follows into the following capacitor circuit.



Derive an expression for $v_{out}(t)$ in terms of $I_s(t)$, C, and t when under **constant** light exposure ($I_s(t) = 5$ nA). Then, find the capacitor value C such that, after 1 hour under exposure, the capacitor voltage is $V_{out} = 5$V. The initial voltage on the capacitor is 0V.

Solution: The charge on a capacitor is defined through the equation $C = \frac{Q}{V}$, and so the current being applied ($I = dQ/dt$) to a capacitor follows by taking the time-derivative of the capacitor equation $I = \frac{dQ}{dt} = C\frac{dV}{dt}$. This can be rearranged to find V in terms of the current source and the capacitor value:

$$\frac{dV_{out}}{dt} = \frac{1}{C}I_s(t) \implies \int_0^t \frac{dV_{out}(t')}{dt'}dt' = \frac{1}{C}\int_0^t I_s(t')dt' \implies V_{out}(t) = \frac{1}{C}\int_0^t I_s(t')dt' + V_{out}(0).$$

Since there is no initial voltage across the capacitor at $t = 0$, we can simplify our final solution to

$$V_{out}(t) = \frac{1}{C}\int_0^t I_s(t')dt'.$$

Since we are looking for $V_{out}(t)$ when under constant sun exposure, we can substitute the constant value $I_s(t) = 5$nA into the integral. This yields

$$V_{out}(t) = \left(\frac{5 \times 10^{-9}\ \text{A}}{C}\right) t$$

To determine the capacitance C needed to meet our voltage condition, we first recognize that the voltage expression simplifies thanks to the photodetector behaving like a constant current source

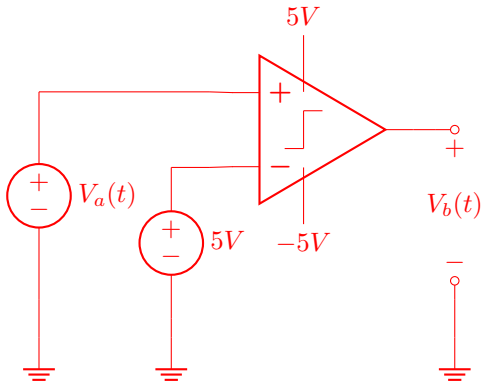
$$V_{out}(t) = \left(\frac{1}{C}\right) I_s t \implies C = \frac{(5 \times 10^{-9}\ \text{A})(60 \times 60\ \text{s})}{5\ \text{V}} = 3600 \times 10^{-9} \left(\frac{\text{A s}}{\text{V}}\right).$$

Thus $C = 3.6\mu$F.

2. [6 pts] We would like to also use the circuit above in part 1 to power a separate LED device that indicates the state of sun exposure on our plant. The device indicates sufficient sun exposure when +5V is applied across it, and conversely indicates the plant is critically underexposed, or dying, when −5V is applied across it. Design a circuit using a comparator that outputs +5V once the plant has received at least 1 hour of full exposure, and otherwise outputs −5V. You have a voltage source $V_a(t)$ which corresponds to $V_{out}(t)$ from part 1.

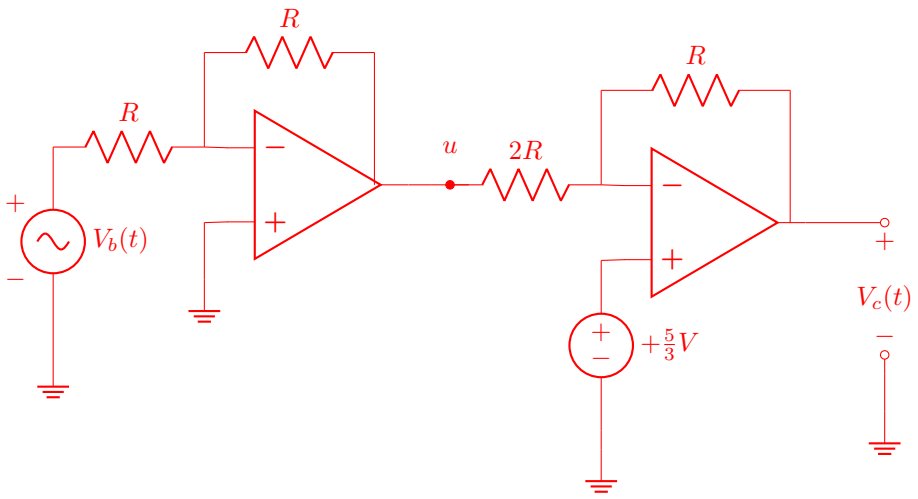
   Regardless of your answer in part 1 assume that $V_a(t)$ functions exactly as previously described; so $V_a(t) = 5\text{V}$ after an hour of full exposure. You may use as many voltage sources as you would like. Label the comparator rails and any voltage sources you include (with explicit voltage values).

   Solution: From part 1), $V_a(t)$ is directly proportional to the exposure time. Therefore $V_a(t)$ will output $5V$ after the sensor has been exposed for 1 hour and less than 5V otherwise. By putting a voltage of 5V in the negative terminal of the op-amp, −5V will output until 1 hour is reached.



3. [6 pts] We want to use the comparator output from the previous circuit to communicated with our ESP32 microcontroller. However, the ESP32 can only read 0V to 5V, instead of the −5V to 5V output voltage from the comparator in part 2. Furthermore, you do not have access to any other comparator. Design a circuit, without using a comparator, that scales and shifts an input voltage in the range 5V $\leq V_{in} \leq$ +5V to produce an output voltage 0V$\leq V_{out} \leq$ +5V. Use the voltage source $V_{in} = V_b(t)$ to model the output of part (2). You are limited to only use circuit elements provided with your lab, which entails 4 resistors, two op-amps, and one constant voltage source. For any resistors or voltage sources that you use in your design, you may pick any component value, but please clearly label and specify its value.

   Solution: Ultimately we would like to assemble a circuit which performs the following voltage map: $V_c(t) = \frac{1}{2}V_b(t) + \frac{5}{2}V$. We need to implement 2 inverting amplifiers with an additional voltage source. Inverting the input voltage $V_b(t)$ to $-V_b(t)$ is first, then scale and shift the output using another inverting amplifier.



The first stage simply inverts $V_b(t)$ since the output at node u is

$$u = 0 - R\left(\frac{V_b - 0}{R}\right) = -\frac{R}{R}V_v(t) = -V_b(t)$$

Now the output from the second stage produces

$$V_c(t) = \left(\frac{5}{3}V\right) - \frac{R}{2R}\left(u - \frac{5}{3}V\right) = \left(\frac{5}{3}V + \frac{5}{6}V\right) + \frac{1}{2}V_b(t) = \frac{1}{2}V_b(t) + 2.5V$$

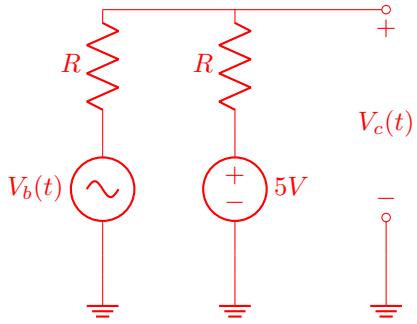
Thus, our circuit reproduces the correct mapping of the $V_b(t)$ input voltage.

Note: Mapping one voltage range to another using linear circuit components always results in a unique affine transformation determined by the endpoints. Hence, if we seek $[-5, +5] \mapsto [0, 5]$ and we only are allowed linear components and no comparators, we must have some scaling and shifting involved. We can do this

$$V_c = aV_b + b, \ a \text{ is the slope and } b \text{ is the offset}$$

On the lower end we want $V_b = -5 \to V_c = 0$ so $0 = -5a + b$. On the upper end we have $V_b = +5 \to V_c = 5$. so $5 = 5a + b$. Solving these 2 equations we get $a = 1/2$ and $b = 5/2$.

ALTERNATIVE SOLUTION: Since the question states that you are limited using only circuit elements in the lab, it is not necessary to actually use op-amps. A simpler solution would be to use a voltage summer



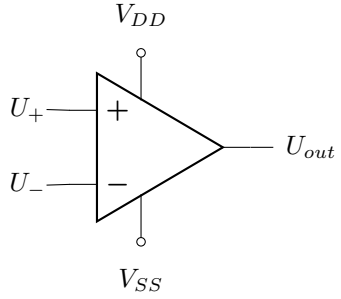
By setting the two resistors equal in value (they can be any resistance), we produce a circuit which outputs the desired map (which follows from a quick super-position assessment)

Appendix A: Op-amp and Comparator Fundamentals

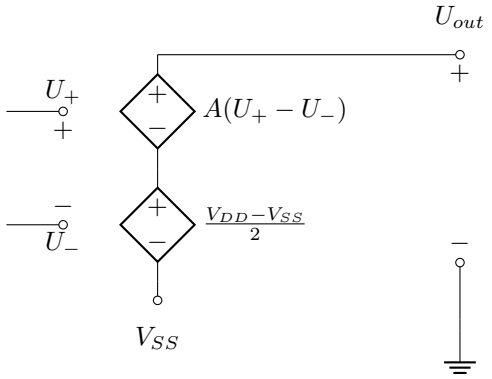
In this section, we will go over a new circuit component called an op-amp. For those of you who have taken ME100, this will be a review. For most, this section will also introduce the comparator, which can be made using an op-amp – something that compares two voltages and indicates which is larger.

Op-amp Model

By definition, an amplifier is something that can transform something small into something much bigger. For example, a speaker is an audio amplifier — if you connect your smart phone to a speaker, it can generate sounds much louder than your phone can. An **op-amp (operational amplifier)** is a device that transforms a small voltage difference into a very large voltage difference. The circuit symbol for an op-amp is shown below:



An op-amp has two input terminals marked (+) and (−) with potentials U_+ and U_-, two power supply terminals called V_{DD} and V_{SS}, and one output terminal with potential U_{out}. The internal circuit design of an op-amp is beyond the scope of this course (if you are curious, you can search for schematics online), but we can model the op-amp with the following circuit:



This circuit includes two voltage-controlled voltage sources. (Note that the dependent voltage sources in the schematic above are referenced to V_{SS}, not ground.) The bottom voltage source adds the voltage $\frac{V_{DD}-V_{SS}}{2}$ so that when $U_+ = U_-$, the output voltage is the midpoint between V_{DD} and V_{SS}. The top source creates a voltage $A(U_+ - U_-)$, which amplifies the difference between the two input terminals. This is commonly known as the op-amp gain.

In a good op-amp, the constant A is very large — approaching infinity. If A is very large, does the op-amp produce infinite voltage? It might seem like this is the case from the equivalent circuit schematic, but the op-amp's power must come from somewhere – it comes from the supply voltages V_{SS} and V_{DD}. This means that U_{out} cannot be greater than V_{DD} or less than V_{SS}.

Following the schematic given above, the behaviour of an op-amp can be summarized with the equation

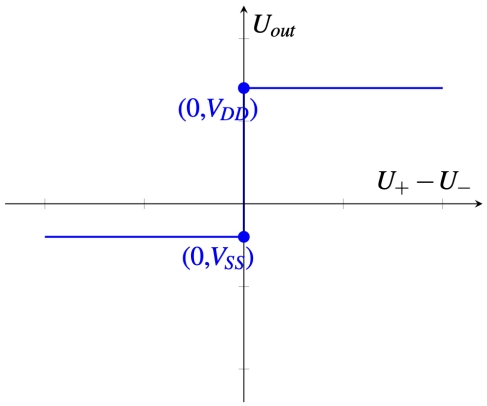
$$U_{out} = A(U_+ - U_-) + \frac{V_{DD} + V_{SS}}{2}$$

except U_{out} cannot be above V_{DD} or below V_{SS}. So U_{out} is actually given by the following equation, where the first and third cases are the cutoffs:

$$U_{out} = \begin{cases} V_{SS} & A(U_+ - U_-) + \dfrac{V_{DD} + V_{SS}}{2} < V_{SS} \\ A(U_+ - U_-) + \dfrac{V_{DD} - V_{SS}}{2} & V_{SS} \leq A(U_+ - U_-) + \dfrac{V_{DD} + V_{SS}}{2} \leq V_{SS} \\ V_{DD} & V_{DD} < A(U_+ - U_-) + \dfrac{V_{DD} + V_{SS}}{2} \end{cases}$$

Op-amps as Comparators

For very large A (close to infinity), the non-clipped output $A(U_+ - U_-) + \frac{V_{DD}+V_{SS}}{2}$ is infinity if $U_+ - U_- > 0$, and negative infinity if $U_+ - U_- < 0$. Then, we are always in either the first or third case, which gives us the following plot:

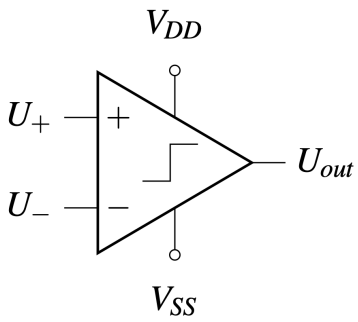


Since A is very large, there is a very sharp transition in the center of the plot. Therefore, when $U_+ < U_-$ (or equivalently, when $U_+ - U_- < 0$), then U_{out} equals V_{SS}. Similarly, when $U_+ > U_-$, then U_{out} equals V_{DD}. In this case, the op-amp is acting as a comparator since it indicates which voltage (U_+ or U_-) is larger, even if the difference between them is very small.

Comparators in Practice

In practice, circuit designers rarely use op-amps to compare inputs but instead use special components called *comparators*. As demonstrated above, op-amps can function as comparators; however, they are rather slow and imprecise since they're optimized for signal amplification with output voltages always staying between the rails. Dedicated comparators, by contrast, are designed to output only the supply voltages and are preferred to op-amps for their faster operation. The plot of input and output voltages for a comparator is identical to that of an ideal op-amp in the comparator configuration, shown in the previous subsection.

The circuit symbol for a comparator is shown below:



Appendix B: Significant Figures

There are two kinds of numbers in the world:

1. **Exact**: There are exactly 12 eggs in a dozen.
2. **Inexact**: any measurement. If I quickly measure the width of a piece of notebook paper, I might get 220 mm (2 significant figures). If I am more precise, I might get 216 mm (3 significant figures). An even more precise measurement would be 215.6 mm (4 significant figures).

Accuracy refers to how closely a measured value agrees with the correct value. **Precision** refers to how closely individual measurements agree with each other.

Significant figures convey the precision of a measured or reported value. The following rules define how to determine the number of significant figures in a number.

Rule 1: Non-zero digits

All non-zero digits are **significant**.

- Example: 33.2 has **three** significant figures.

Rule 2: Zeros between non-zero digits

Zeros located between two non-zero digits are **significant**.

- Example: 2051 has **four** significant figures. The zero lies between 2 and 5.

Rule 3: Leading zeros

Leading zeros are **not significant**. They act only as placeholders.

- Example: 0.54 has **two** significant figures.
- Example: 0.0032 has **two** significant figures.

Rule 4: Trailing zeros to the right of a decimal

Trailing zeros to the right of a decimal point are **significant**.

- Example: 92.00 has **four** significant figures.

Note that 92.00 is not equivalent to 92. A measurement of 92.00 mL indicates precision to the nearest 0.01 mL, whereas 92 mL indicates precision only to the nearest 1 mL. Zeros represent real information and cannot be added unless they are known to be significant.

Rule 5: Trailing zeros in whole numbers with a decimal shown

Trailing zeros in a whole number are **significant** if a decimal point is explicitly shown.

- Example: 540. has **three** significant figures.

Rule 6: Trailing zeros in whole numbers without a decimal

Trailing zeros in a whole number with **no decimal shown** are **not significant**.

- Example: 540 has **two** significant figures.

Rule 7: Exact numbers

Exact numbers have an **infinite** number of significant figures. These arise from definitions or counting.

- Example: 1 meter = 1.00 meter = 1.0000 meter = ...

Rounding Example

Round 1000.3 to four significant figures.

- The number 1000.3 has **five** significant figures (the zeros lie between non-zero digits).
- Dropping the final digit ($3 < 5$), we obtain 1000.

The trailing decimal is required to indicate that the zeros are significant. Writing 1000 would imply only **one** significant figure.

Rule 8: Scientific notation

For numbers written in scientific notation,

$$N \times 10^x,$$

all digits in N are **significant**. The exponent and the base 10 are **not significant**.

- Example: 5.02×10^4 has **three** significant figures.

Manipulating Significant Figures

Scientific notation allows explicit control over the number of significant figures.

- 1100 has **two** significant figures.
- 1100. has **four** significant figures.
- 1.10×10^3 has **three** significant figures.